|  |  |  |
| --- | --- | --- |
| Unit | signals from units | Control signals |
| ALU | N, C, Z, result | C1-c4, ALUop |
| RF | Rd1\_data, rd2\_data | Wr\_en, rd\_addr1, rd\_addr2, wr\_addr |
| DM | dm\_data | W\_en, r\_en, addr |
| PM | instruction | addr |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instr | Stage | ALU(ALUop, C4-C1) | RF(C6) | DM(read\_en, wr\_en) | PM(Instr\_addr) |
| ADD | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 1000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| ADDI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 1001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| SUB | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 1110 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| SUBI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 1111 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| AND | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 010, 1000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| ANDI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 010, 1001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| OR | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 011, 1000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| ORI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 011, 1001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| XOR | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 100, 1000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| XORI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 100, 1001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| LSH | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 101, 1000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| LSHI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 101, 1001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| ASH | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 100, 1000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| ASHI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 100, 1001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| CMP | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 1110 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 0 |  |  |
| CMPI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 1111 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 0 |  |  |
| MOV | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 0000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| MOVI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 001, 0001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| LUI | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 010, 1001 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |
| LOAD | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 010, 1000 |  |  |  |
|  | MEM |  |  | 1,0, rsrc |  |
|  | WB |  | 1, rdest |  |  |
| STOR | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 010, 1000 |  |  |  |
|  | MEM |  |  | 1,1, rsrc, result |  |
|  | WB |  | 1, rdest |  |  |
| Bcond | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 000, 0000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 0 |  |  |
| Jcond | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 000, 0000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 0 |  |  |
| JAL | Overall |  |  |  | instr\_addr |
|  | RD |  | rsrc, rdest |  |  |
|  | EXE | 000, 0000 |  |  |  |
|  | MEM |  |  | 0,0 |  |
|  | WB |  | 1, rdest |  |  |